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| Cases | Input (I) | Output (D) |
| A | 0000 | 0000000000000001 |
| B | 0001 | 0000000000000010 |
| C | 0010 | 0000000000000100 |
| D | 0011 | 0000000000001000 |
| E | 0100 | 0000000000010000 |
| F | 0101 | 0000000000100000 |
| G | 0110 | 0000000001000000 |
| H | 0111 | 0000000010000000 |
| I | 1000 | 0000000100000000 |
| J | 1001 | 0000001000000000 |
| K | 1010 | 0000010000000000 |
| L | 1011 | 0000100000000000 |
| M | 1100 | 0001000000000000 |
| N | 1101 | 0010000000000000 |
| O | 1110 | 0100000000000000 |
| P | 1111 | 1000000000000000 |

In the 4 to 16 decoder, a signal is outputted from one of the 16 outputs which is determined by the input I. For example, if I = 1101, a signal would be outputted from D(13). This determines which of the 15 temp registers is accessed when writing data. Output D(0) is used as part of the load logic for the other 32 registers.